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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,894	12/08/2003	Herman Kwong	57983.000155	9607

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EXAMINER	
ROSSOSHEK, YELENA	
ART UNIT	PAPER NUMBER
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/728,894	KWONG ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-14* is/are allowed.

6)☒ Claim(s) *1-3, 6-9, 15-18* is/are rejected.

7)☒ Claim(s) *4 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/728,894 filed 12/08/2003 and amendment filed 06/30/2009.

2. Claims 1-18 remain pending in the Application.

3. Applicant's arguments have been fully considered but they are not persuasive.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-3, 6-9, 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hauser et al. (German Patent DE19922186) in view of Agrawal et al. (US Patent 6,184,713).

With respect to claim 1 Hauser et al. teaches a method for mapping contacts of a programmable logic device (PLD) to contacts of an electronic component in a signal routing device having one or more layers (within several IC chips realized on circuit boards/signal routing device and connected one to another or to other electronic components, wherein circuit board includes several layers (Page 1)), the method comprising:

assigning a set of one or more contacts of the PLD to one or more respective contacts of the electronic component based at least in part on a pattern of electrically conductive traces routed from respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device, the one or more channels being formed by arranging vias for contacts of at least the electronic component in the signal routing device (within pin/set of contacts assignment/allocation of the IC chips for connecting one to another within conductor tracks/conductive traces, wherein connection is implemented through corresponding vias in the corresponding layers, and wherein vias form channels (Page 1)).

However Hauser et al. lacks the specifics regarding programmable logic devices (PLD) connected to electronic components. Agrawal et al. teaches CPLD coupled to other circuits/electronic components by PCB traces as shown on the Fig. 1 (col. 11, ll.12-17). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used Agrawal et al. to teach the specifics subject matter Hauser et al. does not teach, because a robust CPLD architecture has been disclosed

for efficiently adapting to the control overhead needs, pinout needs and speed requirements of designs (col. 40, ll.13-18).

With respect to claim 15 Hauser et al. teaches a signal routing device having one or more layers (within circuit board on which several IC chips are assembled (Page1)), and further comprising

an electronic component having a plurality of contacts (within IC chip shown on the Figs. 1-9 (Page 1));

a programmable logic device (PLD) having a plurality of contacts (within IC chip shown on the Figs. 1-9 (Page 1)); and

a plurality of electrically conductive traces connecting contacts of the PLD to respective contacts of the electronic component, the plurality of electrically conductive traces routed from the respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device (within multiple conductor tracks/conductive traces used for connecting several IC chips realized on PCB within channels formed on the board using vias (Page 1));

wherein the one or more contacts of the PLD are assigned based at least in part on a pattern formed by the electrically conductive traces routed from the respective contacts of the electronic component via the one or more channels, wherein the one or more channels being formed by arranging vias for contacts of at least the electronic component in the signal routing device (within pin/set of contacts assignment/allocation of the IC chips for connecting one to another within conductor tracks/conductive traces,

wherein connection is implemented through corresponding vias in the corresponding layers, and wherein vias form channels (Page 1)).

However Hauser et al. lacks the specifics regarding programmable logic devices (PLD) connected to electronic components. Agrawal et al. teaches CPLD coupled to other circuits/electronic components by PCB traces as shown on the Fig. 1 (col. 11, ll.12-17). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used Agrawal et al. to teach the specifics subject matter Hauser et al. does not teach, because a robust CPLD architecture has been disclosed for efficiently adapting to the control overhead needs, pinout needs and speed requirements of designs (col. 40, ll.13-18).

With respect to claims 2-3, 6-9 and 16-18 Hauser et al. teaches

Claim 2: further comprising the step of forming electrically conductive traces between the set of one or more contacts of the PLD and the respective contacts of the electronic component accordance with the pattern of electrically conductive traces (Page 1);

Claim 3: wherein one or more of the electrically conductive traces are routed to respective contacts of the PLD via one or more channels formed at one or more layers of the signal routing device (Page 1);

Claim 6: further comprising the step of: assigning one or more contacts of the PLD to one or more respective contacts of a second electronic component of the signal routing device based at least in part on a pattern of electrically conductive traces routed

from respective contacts of the second electronic component via one or more channels formed at one or more layers of the signal routing device (Page 1);

Claim 7: further comprising the step of: assigning one or more contacts of a second PLD to one or more respective contacts of the electronic component based at least in part on a second pattern of electrically conductive traces routed from respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device (Pages 1, 5).

However Hauser et al. lacks the specifics regarding programmable logic devices (PLD) connected to electronic components. Agrawal et al. teaches CPLD coupled to other circuits/electronic components by PCB traces as shown on the Fig. 1 (col. 11, ll.12-17). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used Agrawal et al. to teach the specifics subject matter Hauser et al. does not teach, because a robust CPLD architecture has been disclosed for efficiently adapting to the control overhead needs, pinout needs and speed requirements of designs (col. 40, ll.13-18).

With respect to claims 8, 9, 16-18 Agrawal et al. teaches:

Claims 8 and 16: wherein the one or more contacts of the PLD are assigned to the respective contacts of the electronic component by programming the PLD (col. 11, ll.12-17);

Claims 9, 17: wherein the electronic component includes one of a group consisting of: a programmable logic device (PLD) and an application specific integrated circuit (ASIC) (col. 11, ll.12-17);

Claim 18: wherein the electrically connective traces are routed to the respective contacts of the PLD via one or more channels formed at one or more layers of the signal routing device (col. 11, ll.12-17).

Allowable Subject Matter

7. Claims 4, 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach determining first pattern of electrically conductive traces routed from respective contacts of the electronic component via at least one channel of the one or more channels; determining a contact assignment pattern for one or more contacts of the PLD based at least in part on the first pattern of electrically conductive traces; refining the first pattern of electrically conductive traces based at least in part on the first contact assignment pattern to generate a second pattern of electrically conductive traces routed from the respective contacts of the electronic component via at least one of the one or more channels.

8. Claims 10-14 are allowed for the same reason as claims 4 and 5 are objected to.

Remarks

9. In remarks Applicant argues in substance:

a) respectfully submits that Hauser and Agrawal, either alone or in combination, fail to disclose, or even suggest, a method for mapping contacts of a programmable logic device (PLD) to contacts of an electronic component in a signal routing device

comprising assigning a set of one or more contacts of the PLD to one or more respective contacts of the electronic component based at least in part on a pattern of electrically conductive traces routed from respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device, wherein the one or more channels are formed by arranging vias for contacts of at least the electronic component in the signal routing device, as presently claimed

8. Examiner respectfully disagrees for the following reasons:

With respect to a) Hauser et al. discloses pin allocation/pin assignment/mapping contacts for connecting IC chips with one another and/or connecting single IC chip with other electrical or electronic components, wherein conductor tracks/channels are allocated in multiple layers, and wherein layers of conductor tracks from one wiring layer to another wiring layer are possible by arranging corresponding vias/holes, and for implementation of routing/wiring in the same layer the channels are used. Moreover Agrawal et al. fills the deficit of Hauser et al. by disclosing connection of CPLD with other integrated circuits using PCB traces and assigning I/O pins (col. 11, ll.21-25). Therefore the combination of Hauser et al. and Agrawal et al. read claims 13, 6-9 and 15-18 as currently written, and Examiner maintains rejection of claims 13, 6-9 and 15-18 under 35 USC § 103.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is (571)272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

11/08/2009
HR

/Helen Rossoshek/
Primary Examiner, Art Unit 2825